

**Notice of References Cited**Application/Control No.  
09/977,585Applicant(s)/Patent Under  
Examination  
HOU ET AL.Examiner  
John P TrimmingsArt Unit  
2133

Page 1 of 1

**U.S. PATENT DOCUMENTS**

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
	A	US-6,052,798	04-2000	Jeddeloh, Joseph	714/8
	B	US-5,758,056	05-1998	Barr, Robert C.	714/7
	C	US-6,181,614	01-2001	Aipperspach et al.	365/200
	D	US-5,970,000	10-1999	Kirihata et al.	365/200
	E	US-6,484,277	11-2002	Schonemann, Konrad	714/710
	F	US-6,651,202	11-2003	Phan, Tuan L.	714/733
	G	US-6,493,654	12-2002	Sugimoto, Masaaki	702/185
	H	US-			
	I	US-			
	J	US-			
	K	US-			
	L	US-			
	M	US-			

**FOREIGN PATENT DOCUMENTS**

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	Classification
	N					
	O					
	P					
	Q					
	R					
	S					
	T					

**NON-PATENT DOCUMENTS**

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	"Built-In Self-Repair for Divided Word Line Memory", Shyue-Kung Lu et al., Circuits and Systems, 2001, Vol. 4, pp 13-16, 6-9 May 2001.
	V	"A BISR (Built-In Self-Repair) Circuit for Embedded Memory with Multiple Redundancies", Heon-Cheol Kim et al., IEEE 1999 0-7803-5727-2/99, pp 602-605, 26-27 Oct 1999.
	W	
	X	

\*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)  
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.